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FINAL REPORT

REPAIR OF 16.5 GHz RADAR

DATA PROCESSOR AND

RECEIVER CHASSIS

PREPARED FOR: NASA Manned Spacecraft Center
Houston, Texas 77058

UNDER CONTRACT: NAS 9-11278

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1. INTRODUCTION

The following 16.5 GHz radar chassis were repaired under Contract No. NAS 9-11278 for the NASA Manned Spacecraft Center, Houston, Texas.

(1) Data Processor SM-D-533946N S/N 6

(2) Coherent Oscillator (COHO) (Rcvr) SM-D-533217 S/N 3

(3) Variable Frequency Oscillator (VFO) (Rcvr) SM-D-533220 S/N 3

(4) Preamplifier (Rcvr) SM-D-533835

Repairs were completed on the three receiver chassis and they were returned in October 1970. The processor repair was delayed by the procurement of a matched set of delay lines, which is a long lead item. Processor repairs were then completed and the unit returned in December, 1970.

The following is a brief description of the unit repair requirement:

a. Processor.

(1) Install new delay line matched set and align the associated line driven and post delay amplifiers.

(2) Replace DC amplifier module (MD-16 on 1A6A5).

(3) Modify circuitry to provide simultaneous recording of real antenna aperture video and synthetic aperture video.

(4) Perform electrical realignment.

(5) Performed unit test and documentation of test data.

b. Coherent Oscillator.

(1) Completely rebuild the electronic circuits.

(2) Perform electrical alignment.

(3) Perform unit test and documentation of test data.

c. Variable Frequency Oscillator.

(1) Completely rebuild the electronic circuits.

(2) Perform electrical alignment.

(3) Perform unit test and documentation of test data.

d. Preamplifier.

(1) Replace the signal cable.

(2) Perform electrical alignment.

(3) Perform unit test and documentation of test data.

2. PROCESSOR REPAIRS

a. Equipment Setup. Figure 1 illustrates the general lab test setup for repairs and alignment. The control panel provides an interface between the Data Processor, power supplies and the test equipment. All data processor outgoing signals are terminated at the control panel. Incoming signals are terminated within the data processor. Only one input signal is required for general testing and alignment, the video input pulse which simulates a radar target return.

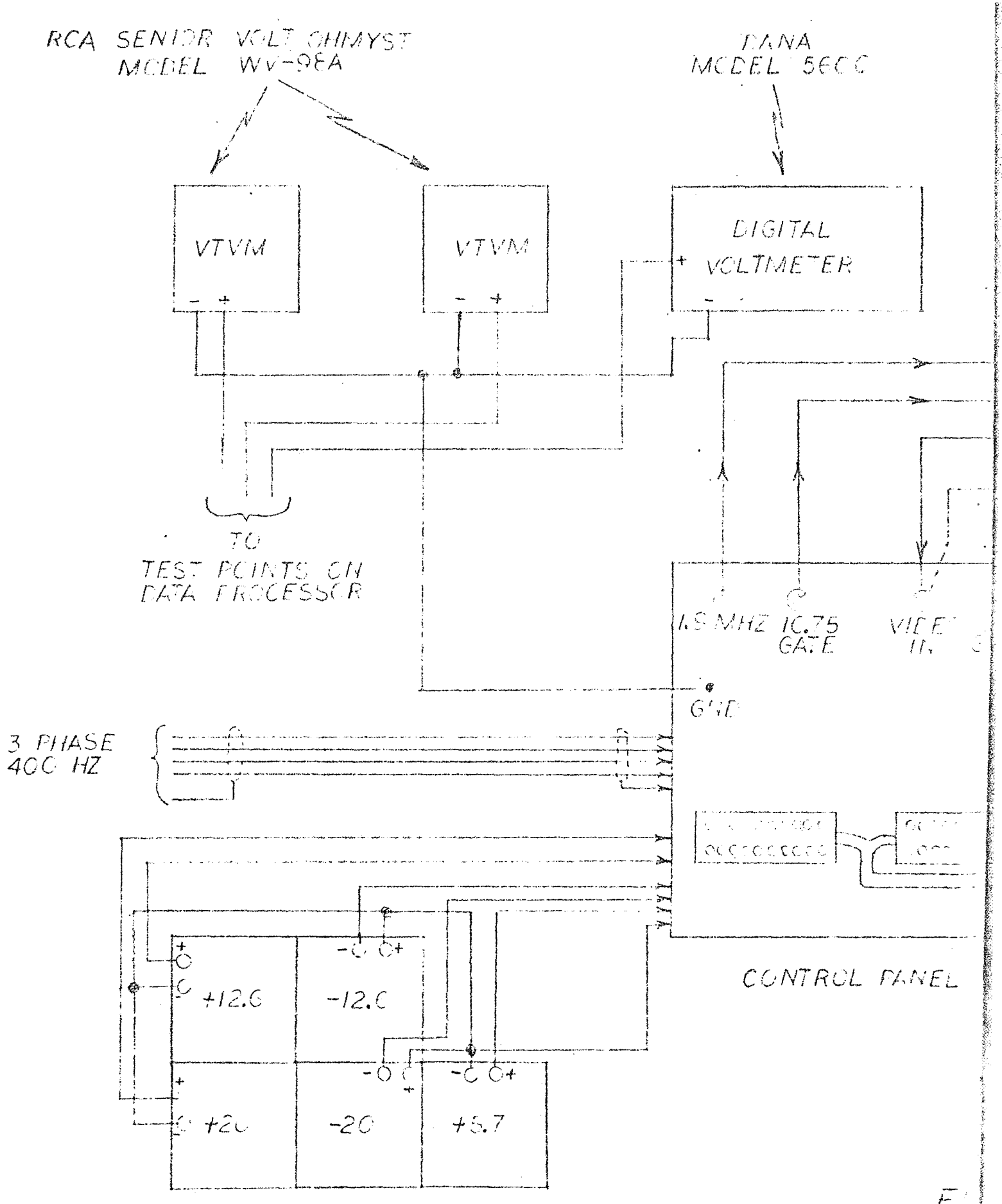
For general testing the video input signal is of plus or minus polarity at a level of one (1) volt O-P maximum and is fed directly to the "video in" connector on the control panel. For measuring feedback factor, the video first passes through the balanced modulator where it is modulated by a low audio frequency (typically 0 - 20 hertz). The frequency counter monitors the 1.91 MHz signal of the signal integrator timing control loop. The volt meters are used to monitor various DC voltages at test points throughout the Data Processor.

b. Description of Repairs.

(1) New interoven assembly (SM-D-533056) which includes a new matched set of delay lines (1) 1072μ sec delay line (SM-D-533061) and (2) 536μ sec delay line (SM-D-533358) was installed in the Data Processor. The associated delay line drivers and post-delay amplifiers were aligned to compensate for irregularities in the delay lines bandpass characteristics.

(2) Install New DC Amplifier. A new DC amplifier was installed to replace MD-16 on timing board A (1A6A6) which was defective. The new DC amplifier module is an improved version which has much better stability than the unit replaced.

(3) Installed New Filter Choke. A new 8.2μh filter choke (L4) was replaced in the +20 V power input line on the filter assembly (1A6A1A1).


RCA SENIOR VOLT OHMYST
MODEL WV-98A
DANA
MODEL 5ECC
VTVM
VTVM
DIGITAL
VOLTMETER
TO
TEST POINTS ON
DATA PROCESSOR
4.5 MHZ
10.75
GATE
GND
3 PHASE
400 HZ
+12.6
-12.6
+20
-20
+5.7
CONTROL PANEL
D.C. POWER SUPPLIES
POWER DESIGNS INC. MODEL 3050-S

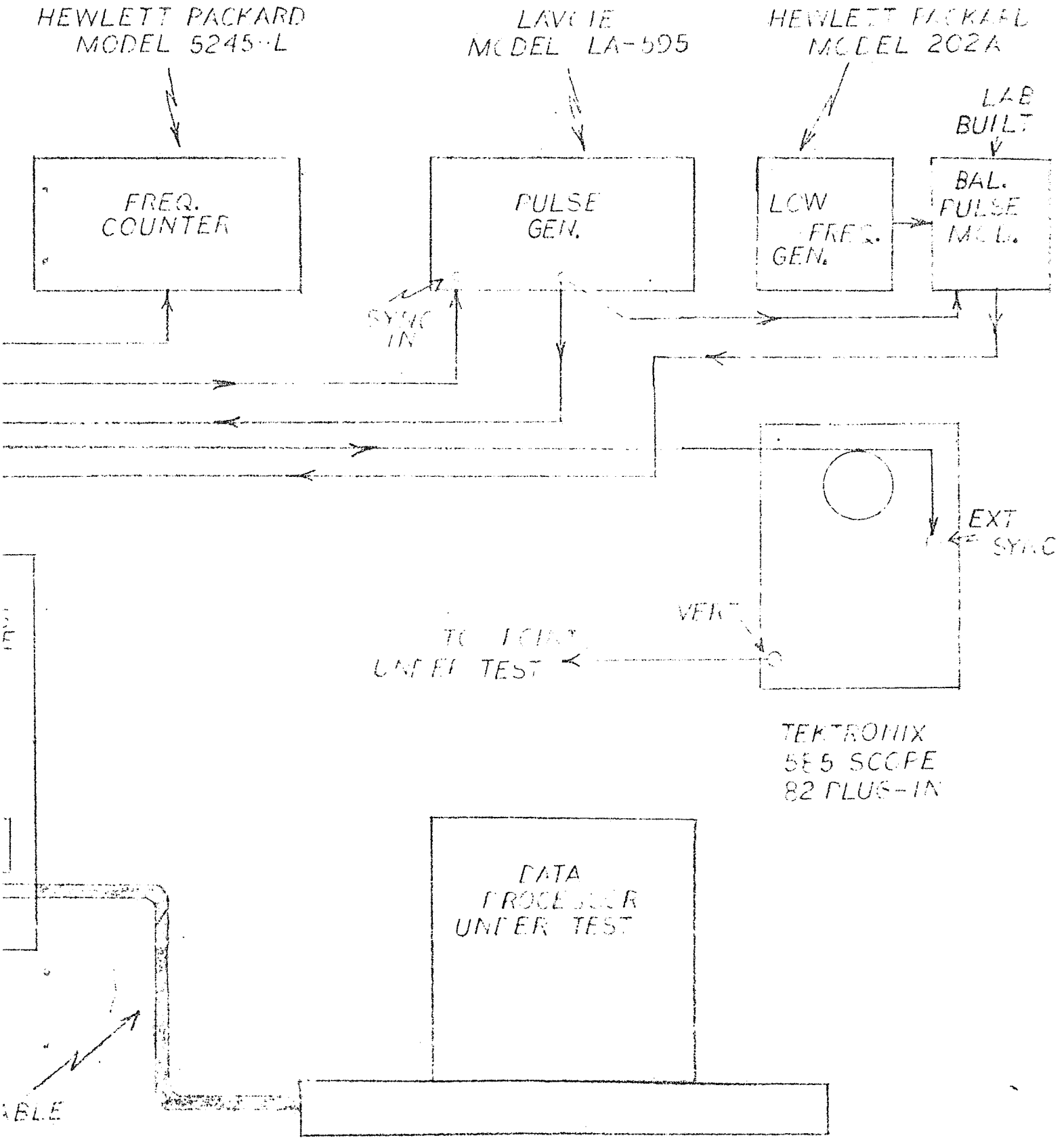


FIGURE 1

DATA PROCESSOR
TEST SET-UP
F. R. GABANY MAR. 27, 1970

(4) · Real-Synthetic Aperture Modification. The Data Processor was modified as outlined In Philco-Ford Document, "Processor Changes for Synthetic-Real Aperture", No. 44231. This modification provides the capability to record real aperture video simultaneously with synthetic aperture video. The real and synthetic aperture video recording is time shared as illustrated by the composite video figure on Drawing No. 44231. A copy of this document is included in the Appendix.

This modification reduces the incoming noncoherent video from 2 volts to 1/2 volt and re-routes the video path to the video compression board (1A6A8). The new switching configuration combines the composite real aperture video and synthetic aperture video on a common path and sends it to the recorder. The video recorder then separates the real and synthetic aperture video and records them on separate film strips.

c. Final Alignment and Test. Final alignment was performed as outlined in "Alignment Procedure - Data Processor - Video Sweep Integrator". Final testing and documentation was performed as specified in "Acceptance Test Plan - Data Processor P/N SM-D-533946N", Philco-Ford document No. 40262.

Both of the above documents are included in the Appendix.

3. RECEIVER REPAIRS

The COHO and VFO chassis normally operate in a common oven on the receiver chassis. Both units were damaged by excessive heat when the oven temperature control failed and the oven power failed to shut off. Since it was not practical to separate damaged and undamaged components, all electrical components were removed from the two chassis and replaced by new units. The defective oven controller was previously replaced in the field.

a. Coherent Oscillator (COHO). The coherent oscillator was damaged by excessive heat, therefore, all electrical components were removed from the chassis. The COHO was then rebuilt using all new electrical components. Electrical test and documentation were performed as outlined in "Acceptance Test Plan, COHO Assy SM-D-533217", Philco-Ford document #40287. This specification which includes the documented test results is included in the Appendix. Figure 2 illustrates the test setup for the COHO test. The Appendix also includes the COHO alignment procedure which was used as a guide for the above alignment and test.

b. Variable Frequency Oscillator (VFO). The variable frequency oscillator was damaged by excessive heat; therefore, all electrical components were removed from the chassis. The VFO was then rebuilt, using all new electrical components. Electrical test and documentation were performed as outlined in

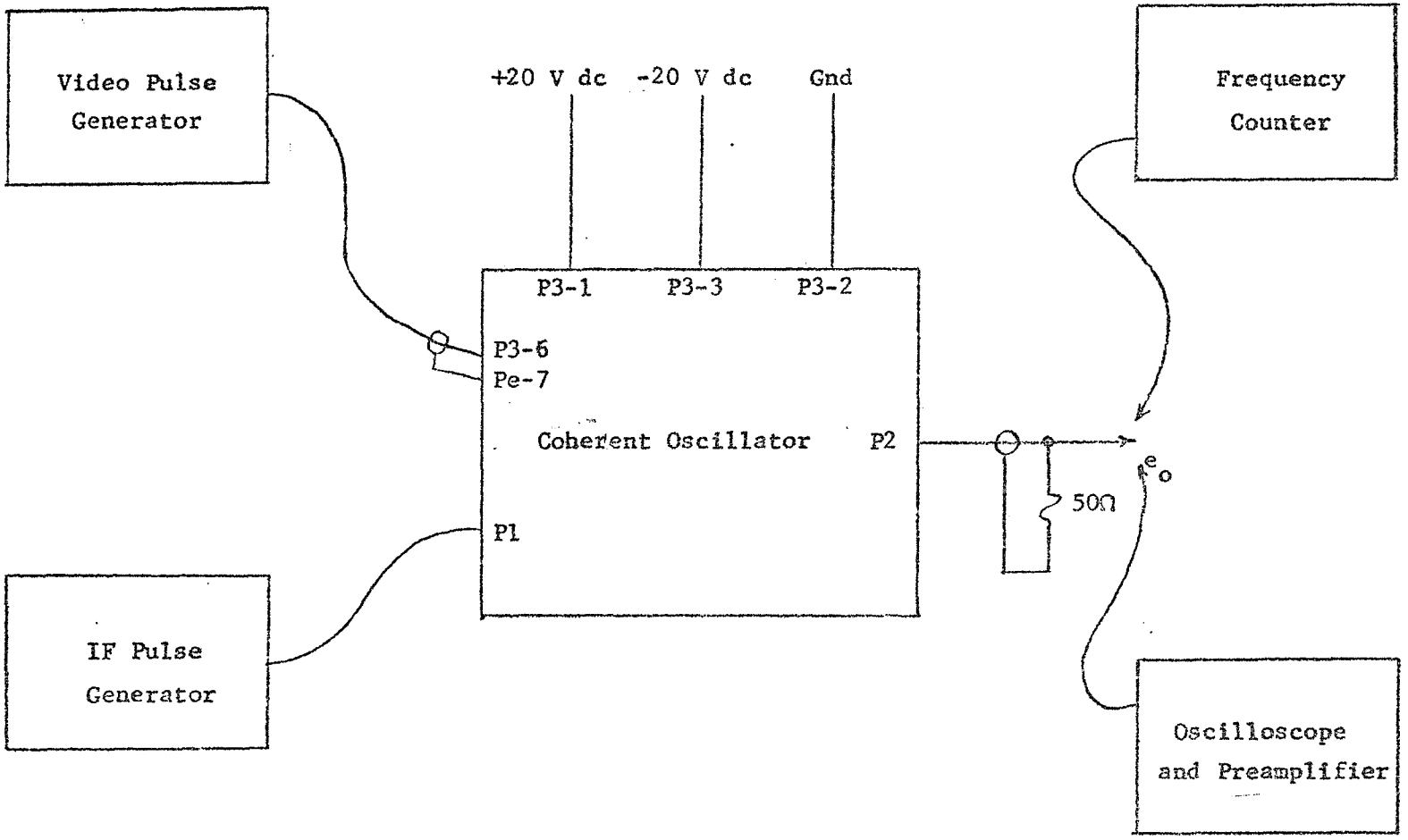


FIGURE 2. TEST SETUP COHERENT OSCILLATOR

"Acceptance Test Plan, VFO Assy. SM-D-533220", Philco-Ford Document No. 40288. This specification which includes the documented test results is included in the Appendix. Figure 3 illustrates the test setup for the VFO test. Figure 4 shows the difference frequency versus control voltage for the VFO which is documented as part of the alignment procedure. The Appendix also includes the VFO alignment procedure which was used as a guide for the above alignment and test.

c. Preamplifier. Repairs for the preamplifier consisted of:

(1) Replacing the signal output coaxial cable and its associated coaxial connectors.

(2) Replacing lost hardware for hold down and polarization on the power connector.

The electrical circuits of the preamplifier were then given a complete realignment. Electrical test and documentation were performed as outlined in "Acceptance Test Plan, Pre-Amp Assy. SM-D-533835", Philco-Ford Document No. 40289. This specification which includes the documented test results is included in the Appendix. Figure 5 illustrates the test setup for the preamplifier test. The Appendix also includes the preamplifier alignment procedure which was used as a guide for the above alignment and test.

4. CONCLUSIONS

The subject Data Processor and three receiver chassis have been repaired, tested and meet their respective original design specifications as documented in this report. The Data Processor was also modified to provide for the simultaneous recording of the synthetic and real aperture video.

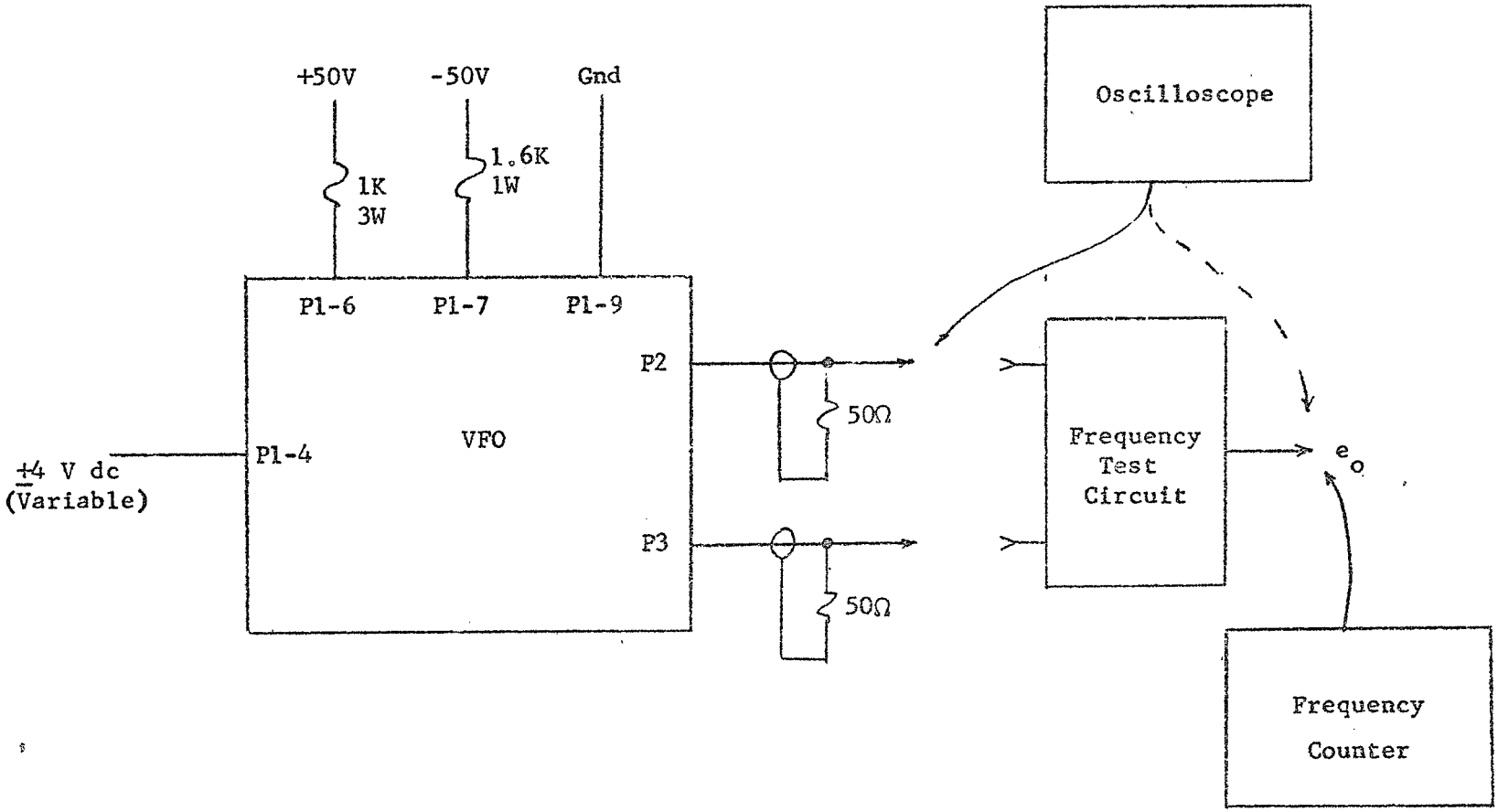


FIGURE 3. TEST CIRCUIT VARIABLE FREQUENCY OSCILLATOR

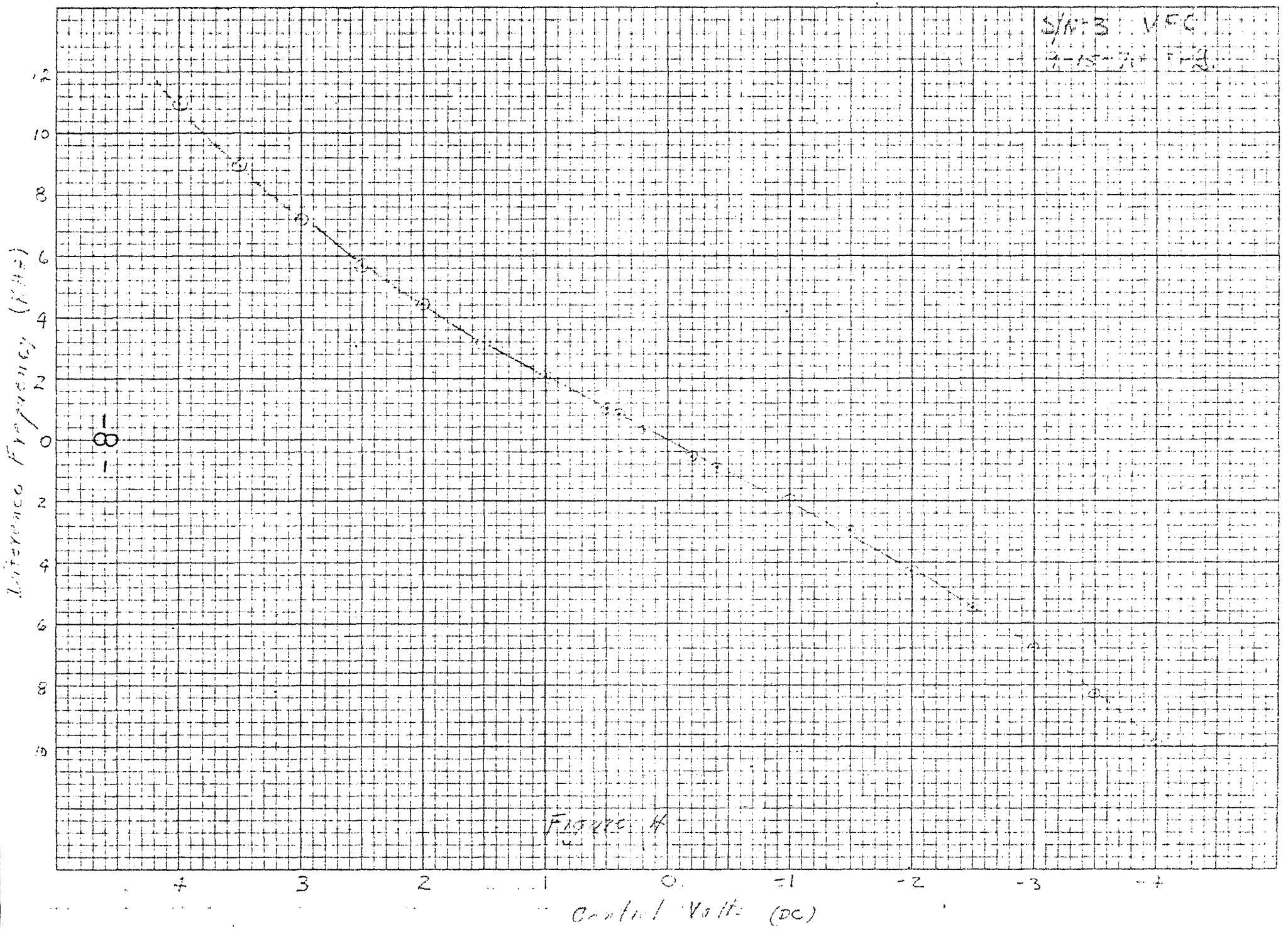


Figure 4

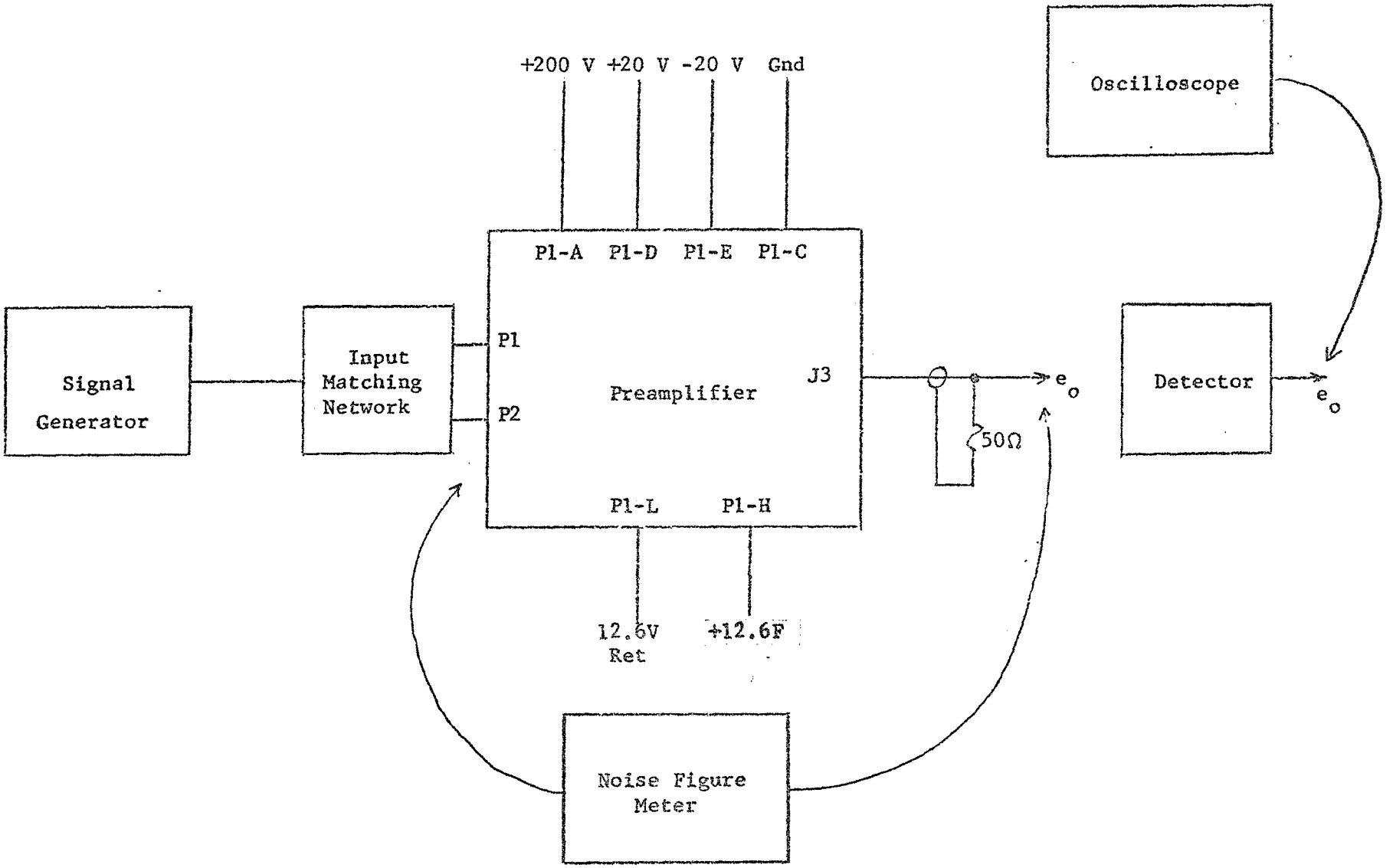


FIGURE 5. TEST CIRCUIT, PREAMPLIFIER

APPENDIX

1. Alignment Procedure - Data Processor Video Sweep Integrator

2. "Acceptance Test Plan Data Processor P/N SM-D-533946N"
   Philco-Ford Document No. 40262

3. Coherent Oscillator Alignment Procedure

4. "Acceptance Test Plan, COHO Assy. SM-D-533217"
   Philco-Ford Document No. 40287

5. Variable Frequency Oscillator Alignment Procedure

6. "Acceptance Test Plan, VFO Assy. SM-D-533220"
   Philco-Ford Document No. 40288

7. Preamplifier Alignment Procedure

8. "Acceptance Test Plan, Pre-Amp Assy. SM-D-533835"
   Philco-Ford Document No. 40289

9. Processor Changes for Synthetic-Real Aperture
   No. 44231

ALIGNMENT PROCEDURE
DATA PROCESSOR
VIDEO SWEEP INTEGRATOR
(BOARD 1A6A5)

I. EQUIPMENT REQUIRED:

(A) Oscilloscope (Tektronix Type 585 W/Type 82 Plug-In, or equivalent)
(B) Pulse Generator (LAVOIE LA575 or equivalent)
(C) VTVM
(D) Oscillator (HP Model 202C or equivalent)
(E) Balanced Pulse Modulator

II. ALIGNMENT:

(A) Check the following DC voltages for proper value at input to Data Processor:

1. +20 VDC $\pm$ 2%
2. -20 VDC $\pm$ 2%
3. +12.6 VDC $\pm$ 2%
4. -12.6 VDC $\pm$ 2%
5. +5.7 VDC $\pm$ 2%

(B) AC Couple a 2.0 volt (p-p) bipolar video signal to Pin (J) of the 1A6A5 board. The pulse width should be approximately 1.0 microsec. See figure 1.

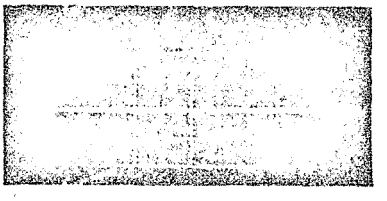


Figure 1

(C) Monitor Pin 5 of MD-3 (40 mc. modulator) with scope. Adjust both the capacitor in MD-3 and resistor R-4 until the 40 mc carrier is nulled. The nulled carrier should not exceed 50 millivolts peak-to-peak. See figure 2.

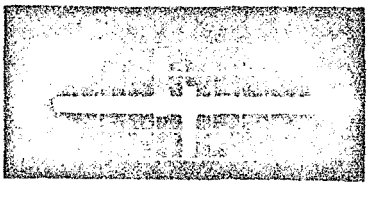


Figure 2

(D) Monitor Pin 2 of MD-7 (input to delay line) with scope. Adjust capacitor in MD-2 (40 mc phase shifters) for 90 degrees of phase shift. A 90 degree phase shift occurs when the sidebands are of equal amplitude. Recheck step (B). See figure 3

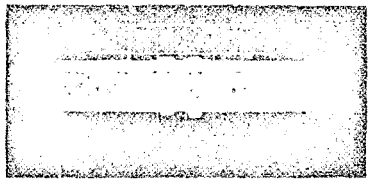


Figure 3

(E) Monitoring the same point as in (C) above observe the degree of phase modulation. If necessary select resistor R-5 for 30 degrees of phase modulation (ratio of peak-to-peak unmodulated carrier to peak-to-peak sidebands equals 0.866). Typical carrier amplitude is 0.25 Vp-p. Recheck step (C).

(F) Remove cable coming back from delay line (P-3). Monitor Pin 5 of MD-11 (40 mc. phase detector) with scope and adjust capacitor in MD-11 for best null. The nulled carrier should be less than 50 millivolts peak-to-peak. Reconnect cable. Typical carrier amplitude is 0.25 Vp-p.

(G) 40 mc Phase Lock:

(1) Short the input of MD-13 (DC amplifier) to ground. Monitoring TP-17 with a DC voltmeter adjust R-8 for a maximum positive voltage, then adjust R-27 to lower the voltage to +2.0 VDC. Now readjust R-8 for a near zero reading. Remove short, the voltage should remain near zero VDC. Typical readings at TP-17 are between $\pm$ 0.5 VDC.

(H) 1.91 mc Timing Loop Lock:

(1) Monitoring TP-8 with a DC voltmeter and adjust R-20 for approximately +2.0 VDC.

(2) Monitor TP-18 with a DC voltmeter and adjust R-21 until limiting at a positive voltage occurs. Then adjust R-11 to lower the voltage to +1.5 VDC.

(3) Monitor TP-18 with a DC voltmeter and adjust R-21 until limiting at a negative voltage occurs. Then adjust R-10 to lower the voltage to -1.5 VDC.

(4) Short Pin 7 of MD-28 to ground (DC Amp). Adjust R-21 for a near zero voltage at TP-18. Remove short.

(5) Short Pin 6 of MD-29 (1.91 oscillator) to ground. Vary capacitor in MD-29 for maximum rise time of the video at TP-19. See figure 4. Remove short and adjust R-21 for maximum video rise time. There should now be no change in the video as Pin 6 of MD-29 is shorted. If the loop does not lock in repeat steps 1 thru 5. If a peak in rise time cannot be observed by adjustment of the MD-29 capacitor it will be necessary to change the 1.91 mc crystal to a different frequency. Record frequency of the locked in 1.91 mc oscillator at TP-7.

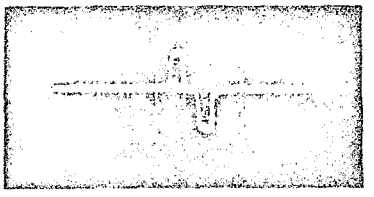


Figure 4

(I) Monitor frequency at TP-7. Adjust R-25 (1.91 mc phase shifter) to both extremes. Determine total frequency excursion then set R-25 to mid range. No further adjustments are necessary if the mid range setting results in a frequency close to that measured in G(5). If not, then adjust R-21 and R-25 to obtain an approximate mid range setting for R-25 at the frequency noted in step G(5).

(J) Feedback Factor Adjustment:

(1) Monitor TP-19 with scope.

(2) AC couple simulated doppler video to Pin (J) of board 1A6A5 (see figure 7). Be careful that limiting of the doppler video does not occur.

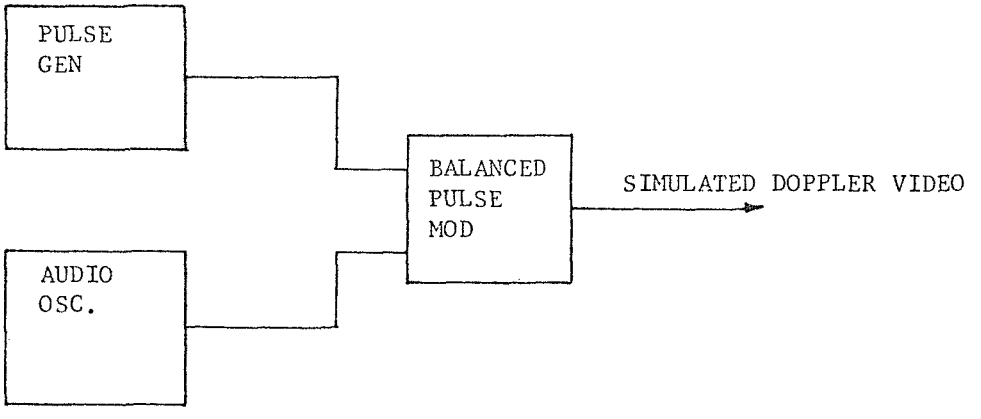


Figure 7

(3) Set modulating frequency to 1.0 cps and record video output at TP-19.

(4) Set modulating frequency to 6.0 cps and adjust R-20 until video is down 3.0 db from preceeding step. This represents a 0.96 feedback factor.

(5) Feedback factor is equal to:

$K = 1 - 6.73 \times 10^{-3}$ fc

where fc = modulating frequency

(6) A typical value for the voltage at TP-8 is $+1.5 \pm 0.05$ VDC.

(7) Repeat steps 3 and 4 making sure that the modulated video amplitude does not change as the modulating frequency is changed.

(K) Sensitivity Adjustment:

(1) Monitor TP-8 with a DC voltmeter.

(2) Break-up loop by actuating loop break-up control and note voltage swing. The voltage should increase to approximately +2.4 volts and then slowly drift back to the value noted in step J(6). If the loop does not lock back in adjust R-19.

Note: If the loop does not lock back in it may be necessary to lower the feedback factor in order to properly set R-19.*

(3) Repeat step (K) until the correct voltage swing is obtained and the loop locks in after being broken up.

(4) Re-adjust feedback factor if necessary.

(L) Monitor TP-19 with scope and adjust capacitor in MD-10 (40 mc phase shifter) and resistor R-8 for balanced video and minimum Beta waveform. See figure 5.

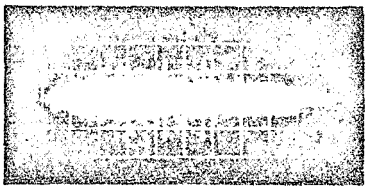


Figure 5

(M) Feedback Factor Overshoot Adjustment:

(1) Monitor TP-8 with a DC voltmeter

(2) Break-up loop by actuating loop break-up control and note voltage swing. Adjust R-28 until the voltage limits at 2.0 VDC. Adjust R-29 until the voltage overshoots the value noted in step J(6) by no more than 50 mv DC. After the loop is broken-up the voltage should stabilize at the value noted in step J(6).

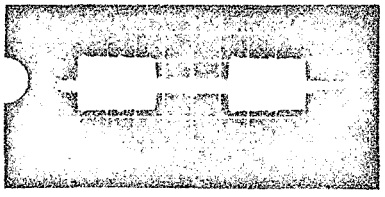
(N) AGE Adjustments:

(1) Adjust R-26 for 1.0 VDC at Pin $\bar{w}$ of board 1A6A5.

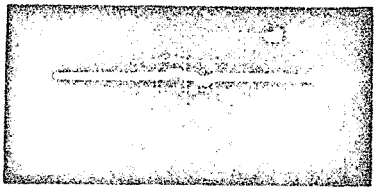
(2) Adjust R-23 for zero VDC when loop is broken-up.

(3) Monitor pin $\bar{p}$ of board 1A6A5 and adjust R-12 for 1.0 VDC.

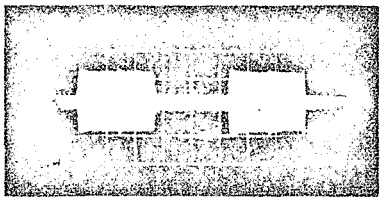
* If R-19 is set so the loop is too sensitive, the loop will not lock in. This can be noted by monitoring the D.C. voltage at TP-8, the voltage will not come low enough to lock loop in (CW decreases sensitivity).



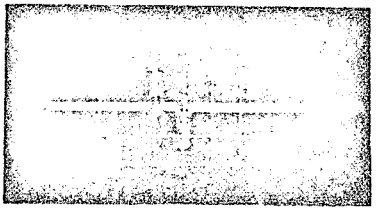
Log Amp Det.
Input
Pin 5 of MD-26
V = 0.5V/cm
H = 0.2 millisec/cm



Low Pass Filter
Output
Pin 3 of MD-15
V = 0.1 V/cm
H = 2.0 microsec/cm



Signal to 1.9 mc
Det.
Pin 3 of MD-31
V = 0.1 V/cm
H = 0.2 millisec/cm



Input to Modulator
Pin 4 of MD-3
V = 0.5 V/cm
H = 2.0 microsec/cm

Figure 6

1.0 General

The inputs and outputs of the data processor are internal to the system with the exception of the AGE and some timing signals for external synchronization of test equipment. On a data processor unit basis, all inputs and outputs are available through the two connectors 1A6A1P1 and 2.

2.0 Test Set-Up

The data processor shall have power applied as follows:

Voltage	Pin No.	Drain (nominal)
Neutral	1A6A1P2-2	100 V-A
120 VAC) ØA)	1A6A1P2-3	260 V-A
400 cps) ØB)	1A6A1P2-4	325 V-A
ØC)	1A6A1P2-5	215 V-A
+20 VDC	1A6A1P1-19	500 MA
-20 VDC	1A6A1P1-37	100 MA
(20V Return)	1A6A1P1-18	---
+12.6 VDC	1A6A1P1-1	2200 MA
-12.6 VDC	1A6A1P1-20	2200 MA
(12.6 V Return)	1A6A1P1-2	---
+5.7 VDC	1A6A1P2-19	700 MA
(5.7 V Return)	1A6A1P2-18	---

3.0 Test Equipment Required

Oscilloscope	Tektronix 585 with Type 82 Plug-in
Pulse Generator	Lavoie LA-595
Counter	Beckman 7370
VTVM	Senior Voltohymst WV-98A
RF Attenuator	Daven Company Type 651-50
Low Freq. Osc.	Hewlett Packard Model 202-C
Balanced Pulse Modulator	(for indication purposes only, calibration not required)

PHILCO
AERONUTRONIC DIVISION

PREPARED BY	DATE	PREPARING ACTIVITY
F.E. Bates	4-25-69	
APPROVED BY	DATE	TITLE OR SUBJECT
		ACCEPTANCE TEST PLAN DATA PROCESSOR, P/N SM-D-533946N
		PROJECT OR MODEL: 1804
		SHEET / DOCUMENT OR REPORT NO.

4.0 Output Signal Specification

With a pre-aligned data processor, the output signals shall be as specified below.

4.1 Timing Waveform Outputs

All timing waveforms are D.C. coupled to an external load of 150 ohms. In addition, the specification on 1) the peak-to-peak amplitude is 1.6 ± 0.3 volts; 2) the maximum amplitude droop is 10%.

4.1.1 536 Gate

The outputs at pins 8, 10, 12 and 14 of 1A6A1P2 shall meet the following specifications:

Period	1072 usec nominal
Duty cycle	50% nominal
Gate rise time	100 nsec max.
Gate fall time	100 nsec max.

NOTE: The positive going portion of the waveform corresponds to the horiz. interval.

4.1.2 268 Gate

The output at pins 21, 23, 25 and 27 of 1A6A1P2 shall meet the following specifications:

Period	536 usec nominal
Duty cycle	50% nominal
Gate rise time	100 nsec max.
Gate fall time	100 nsec max.

4.1.3 140 Gate

The output at pin 29 of 1A6A1P2 shall meet the following specifications:

Period	268 usec nominal
Gate Width (Positive going)	$140.45\ ^{+3.1}_{-0.1}$ usec
Gate Rise Time	100 nsec max.
Gate Fall Time	100 nsec max.

4.1.4 16.75 Gate

The outputs at pins 39, 41, 43 and 45 of 1A6A1P2 shall meet the following specifications:

Gate width	16.75 ± 0.1 usec (50% Amp)
Gate rise time	70 nsec max.
Gate fall time	70 nsec max.
Interpulse period	268 usec nominal
Gate delay (from 268 gate) at 50% points	100 nsec max.

4.1.5 Left Side Gate

The output at pin 37 of 1A6A1P2 shall meet the following specifications:

Period	536 usec nominal
Duty cycle	50% nominal
Gate rise time	1.0 usec max.
Gate fall time	1.0 usec max.
Gate delay (from trailing edge of 16.75 gate)	$123.7\ ^{+3}_{-0}$ usec

NOTE: The positive going portion of this waveform occurs 144 usec after the positive edge of the 536 Gate.

4.1.6 Sweep Shutoff Trigger

The output at pins 31 and 33 of 1A6A1P2 shall meet the following specifications:

Period	268 usec nominal
Pulse width	8 ± 1 usec
Pulse rise time	100 nsec max.
Pulse delay (from 16.75 Gate trailing edge)	$123.7\ ^{+3}_{-0}$ usec

4.1.7 1.9 Mc Oscillator

The output at pin 35 of 1A6A1P2 shall meet the following specifications:

Frequency (cps)	$1{,}911{,}000\ ^{+700}_{-300}$
Pulse rise time	100 nsec max.
Pulse fall time	100 nsec max.
Duty cycle	50% nominal

4.2 Video Signal Outputs

The processor accepts horiz. and vert. video. The inputs are pre-summed and integrated. The respective outputs are horiz. video and vert. video. In addition, the processor will accept Quadrature horiz. video and pre-summed horiz. video. These video inputs will be multiplied and the resultant product will be utilized for Drift Angle Correction (DAC).

4.2.1 Vert. Video

4.2.1.1 When the input on pin 24 of 1A6A1P1 is

Pulse amplitude	Bi-polar +2 ±10% volts peak to peak
Rise time	35 nsec max
Dynamic range	9 ± 0.5 db
Pulse width	1.0 micro-sec nom.

4.2.1.2 The output* on pin 11 of 1A6A1P1 when loaded with 200 Ω shall be:-

4.2.1.2.1 (Video synchronized by 16.75 gate.)

Pulse amplitude**	+0.5V to +1.0V peak
Transfer Characteristic	Shall be capable of variation approximately to the limits as shown in Figure 1 with the adjustments of R10 and R11 for the first break point. R10 and R9 affect one polarity of the bipolar signal and R11 and R12 affect the other polarity of the bipolar signal. (Board 1A6A8)

*The vert. video output occurs during the negative portion of the 536 gate.

4.2.2 Horiz. Video

4.2.2.1 When the input on pin 22 of 1A6A1P1 is:

Pulse amplitude	Bipolar 2 ± 10% Vp to p
Pulse width	1.0 microseconds nominal
Rise time	35 nsec max.
Dynamic range	9 ± 0.5 db

4.2.2.2 The output* on pin 11 of 1A6A1P1 when loaded with 200 Ω shall be:

Pulse Amplitude**	+0.5V to +1.0V peak
Transfer Characteristic	Shall be capable of variation approximately to the limits as shown in Figure 1 with the adjustments of R10 and R11 for the first break point. R10 and R9 affect one polarity of the bipolar signal and R11 and R12 affect the other polarity of the bipolar signal. (Board 1A6A8)

* The horiz. video output occurs during the positive portion of the 536 gate.

** R8 on 1A6A8 may be adjusted for this level.

Feedback factor
0.96 ± .01

For whole video period
horiz. and vert.

NOTE: The method to be used for measuring feedback factor will be:

1. Measure output as in 4.2.2.2 without compression of the output pulse.
2. Multiply input pulse with a low frequency sine wave.
3. Increase frequency until the peak output is 3 db down from that in step 1.

The feedback factor, K, is: $K = 1 - 2\pi\tau f_c = 1 - 6.73 \times 10^{-3} f_c$

where f_c is frequency in step 3
τ is 1072 usec.

4.2.3 D.A.C. Video

4.2.3.1 When the input on pin 22 of 1A6A1P1 is:

Pulse amplitude	+1 ± 10% V peak
Rise time	35 nsec max.
Pulse width	approx. 1.0 us

And the input on pin 4 of 1A6A1P1 is:

Pulse amplitude	26 db below +1 V
Pulse width	approx. 1.0 us
Occurrence time	Simultaneously with the above pulse then:

4.2.3.2 The output on pin 6 of 1A6A1P1 when loaded with 100 Ω to ground shall be:

Pulse amplitude	+0.1 V min.
Rise time	120 nsec max.
Pulse width	approx. 1.0 us

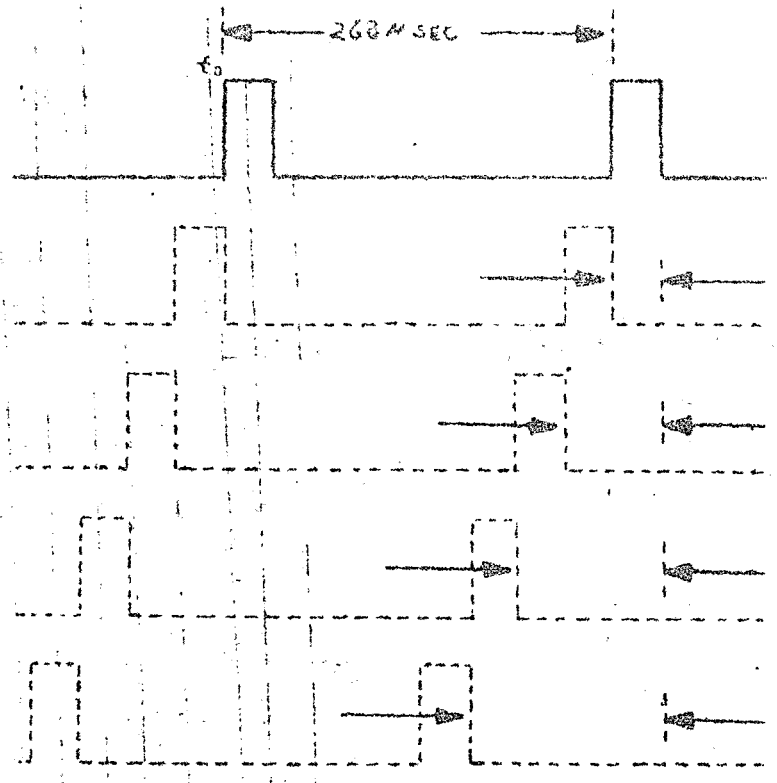
4.2.3.3 Reversing the polarity of one of the above signal pulses will reverse the polarity of the output pulse. The other specifications should remain the same.

4.2.4 Quad Input Output

The output on Pin 6 of 1A6A1P1 should reverse polarity during negative portion of the 268 gate.

4.2.5 Range Swath Selection

The 16.75 gate outputs at Pins 39 & 43 (gates to Transmitter and Receiver) of 1A6A1P2 shall be capable of the following off-sets:



Position #1
Normal Gate (0-10 nautical miles)

Position #2
16.75 μsec ± 5% (1.4 - 11.4 nautical miles

Position #3
33.5 μsec ± 5% (2.7 - 12.7 nautical miles

Position #4
50.25 μsec ± 50% (4.0 - 14.0 nautical miles

Position #5
67.0 μsec ± 5% (5.4 - 15.4 nautical miles

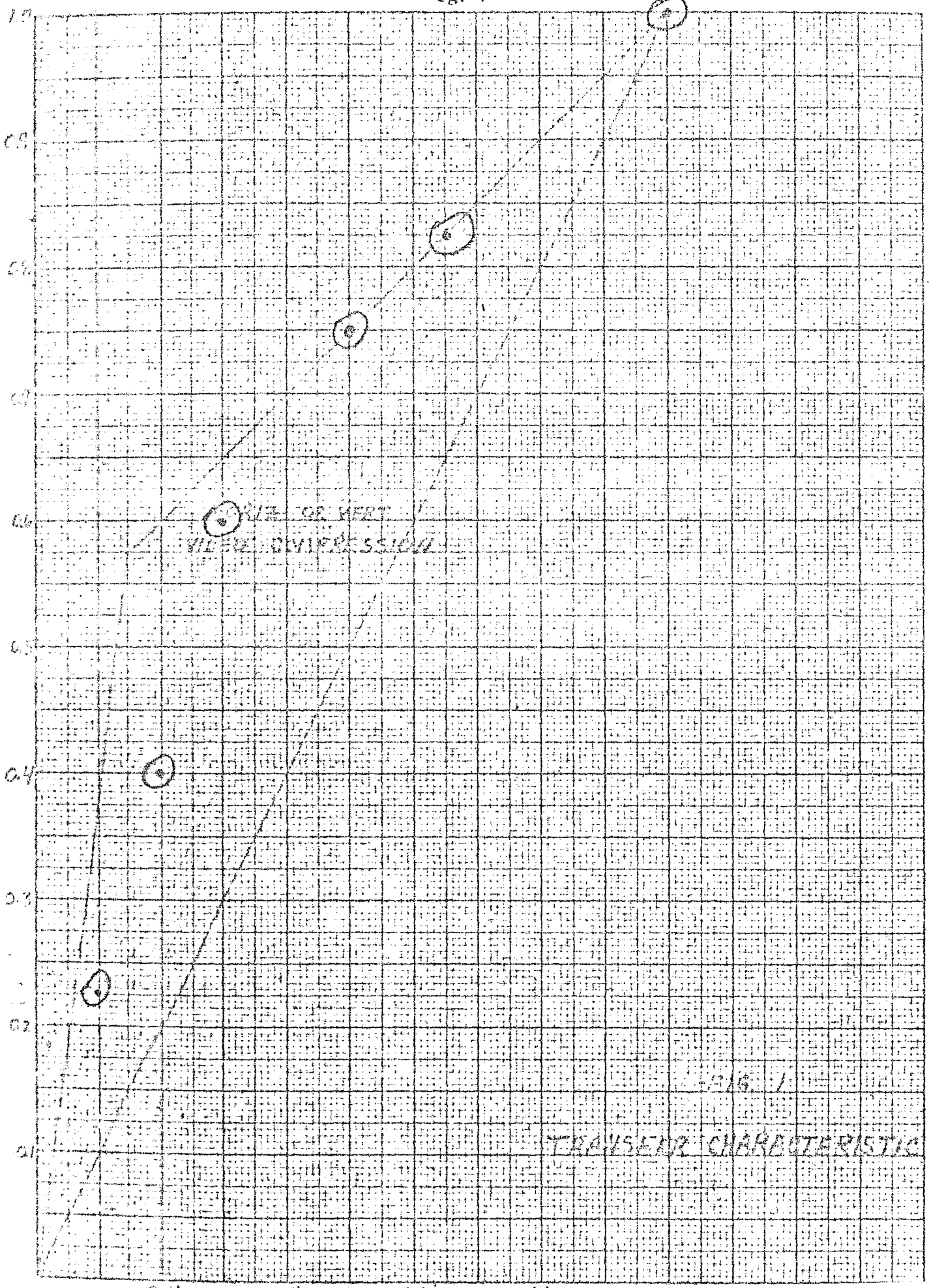


FIG. 1

TRANSFER CHARACTERISTIC

DATA PROCESSOR

Date: 12-6-70

S/N 6

DATA SHEET

Tested by: E P Stabrany

E. L. Richardson/LEC

1.0 Timing Outputs (Para 4.1.1)

			1A6A1P2 PIN NO.			
1.1 536 Gate (para 4.1.1)	Spec.		8	10	12	14
Peak Amplitude	1.6 ± 0.3 volts		1.55	1.5	1.55	1.55
Pulse Droop	10% max.		OK	OK	OK	OK
Rise Time	100 nsec max.		20	20	20	40
Fall Time	100 nsec max.		6	6	8	10
1.2 268 Gate (Para 4.1.2)	Spec.		21	23	25	27
Peak Amplitude	1.6 ± 0.3 volts		1.55	1.4	1.35	1.5
Pulse Droop	10% max.		OK	OK	OK	OK
Rise Time	100 nsec max.		20	18	50	22
Fall Time	100 nsec max.		7	6	8	6
1.3 140 Gate (Para 4.1.3)	Spec.		29			
Peak Amplitude	1.6 ± 0.3 volts		1.35			
Pulse Droop	10% max.		OK			
Gate Width (Positive going)	140.45 $^{+3.1}_{-0.1}$	sec	142.5			
Rise Time	100 nsec max.		28			
Fall Time	100 nsec max.		5			

1.4 16.75 Gate (Para 4.1.4)	Spec	PIN NO. 39	41	43	45
Peak Amplitude	1.6 ± 0.3 volts	1.55	1.6	1.6	1.45
Pulse Droop	10% max.	OK	OK	OK	OK
Gate Width	16.75 ± 0.1 sec	16.75	16.75	16.75	16.75
Rise Time	70 nsec max.	18	18	20	50
Fall Time	70 nsec max.	16	8	20	15
Delay (from 208 Gate)	100 nsec max.	70	70	70	80

1.5 Left Side Gate (Para 4.1.5)	Spec	37	
Peak Amplitude	1.6 ± 0.3 volts	1.55	
Pulse Droop	10% max.	OK	
Rise Time	1.0 μsec max.	40	NANO SEC
Fall Time	1.0 μsec max.	6	NANO SEC
Delay (from trailing edge of 16.75 gate)	123.7 $^{+3}_{-0}$ μsec	124	

1.6 Sweep Shutoff Trigger (para 4.1.6)	Spec	31	33
Peak Amplitude	1.6 ± 0.3 volts	1.5	1.55
Pulse Droop	10% max.	OK	OK
Pulse Width	8 ± 1 μsec	8.2	8.2
Rise Time	100 nsec max.	20	17
Delay (from trailing edge of 16.75 gate)	123.7 $^{+3}_{-0}$ μsec	124	124

1.7 - 1.9 Mc Oscillator (Para 4.1.7)	Spec	35
Rise Time	100 nsec max.	40
Fall Time	100 nsec max.	8
Frequency	1,911,000 $^{+700}_{-300}$ cps	1.910767
Peak Amplitude	1.6 ± 0.3 volts	1.4
Pulse Droop	10% max.	OK

2.0 Video Outputs (Para 4.2) 1A6A1P1

		PIN NO.	
2.1 ~~Sync~~ RAW Video (Para 4.2.1.2)	Spec	11	
Pulse Amplitude (Adjust R8 as required) (Input sync - 16.75 Gate (Para 4.1.4)	+0.5 to +1.0 volts peak		1.0
Rise Time	RECORD		10 NANO SEC
Transfer Characteristic - Figure 1 of Test Procedure			
Adjustment capability			OK

2.2 Horiz Video (Para 4.2.2)	Spec	11	
Pulse Amplitude (Adjust R8 as required)	0.5 -1.0 volts peak		1.0
Rise Time	RECORD		100 NANO SEC
Feedback Factor	0.96 ± 0.01		0.955
Transfer Characteristic - Figure 1 of Test Procedure			
Adjustment capability			OK

2.3 D.A.C. Video (Para 4.2.3)	Spec	6	
Pulse Amplitude	100 mv min.		
Rise Time	RECORD		50 NANO SEC
Output Polarity			

Input #22	#4			
+	+	100	+	100 mv min.
-	-	100	+	100 mv min.
+	-	100	-	100 mv min.
-	+	100	-	100 mv min.

2.4 Quad Output Video (Para 4.2.4)	Spec	6
Video Reverses		OK

3.0 Range Swath Selection (Para 4.2.5)

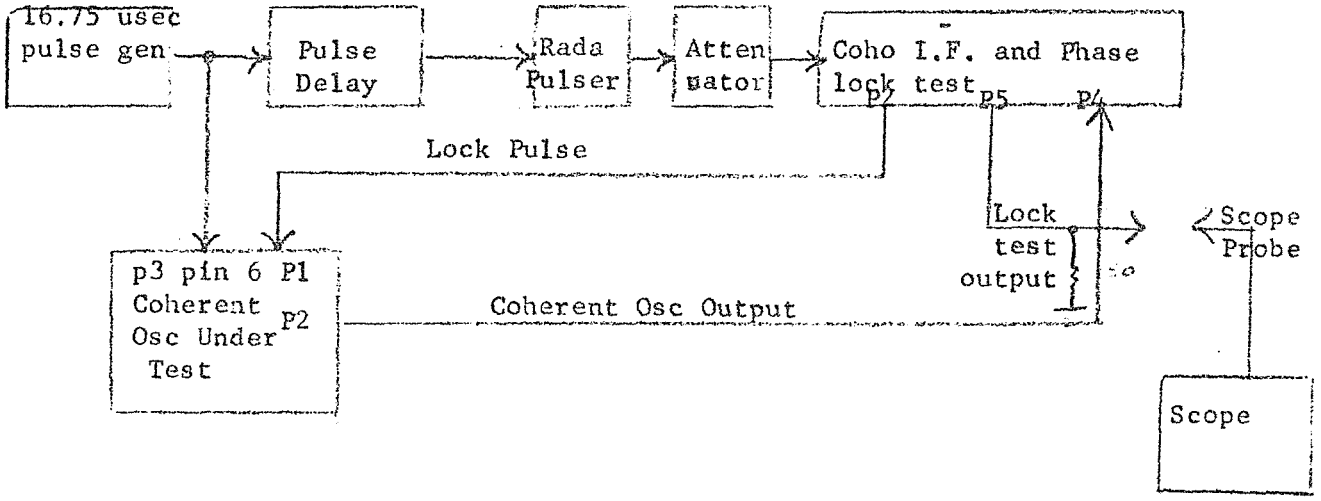
	Spec	Measured Value
Position #1	No Offset	0
Position #2	16.75 usec ± 5%	16.75
Position #3	33.5 usec ± 5%	33.5
Position #4	50.25 usec ± 5%	50.25
Position #5	67.0 usec ± 5%	67.0

TP8	+1.59	V_{DC}
TP14	+0.15	V_{DC}
TP16	-6.8	V_{DC}
TP17	+0.456	V_{DC}
TP18	-0.004	V_{DC}

COHERENT OSCILLATOR (1A4A7)

1. Apply +20 to pin 1, ground to pin 2 and -20V to pin 3 of connector P3.
2. Attach a 360 uuf capacitor temporarily from collector of Q3 to ground to prevent oscillation of the oscillator Q3.
3. Using a Hewlett-Packard 608D signal generator apply .1 V pp 60 Mc signal to connector P1 and by placing a Tektronix type 585 scope from the base of Q2 to ground, adjust first stage Q1 center frequency by adjusting C1 for a maximum as indicated by the scope.
4. Measure the bandwidth and gain of the first stage Q1 and the gain should be approximately 2 and the bandwidth should be greater than 25 Mc.
5. Temporarily disconnect tap of L5 coil from the feedthru to which it is connected. Apply .1 V pp 60 Mc terminated in 50 ohms thru C28 to the last stage Q5 and by means of the scope attached to P2 terminated in 50 ohms adjust C34 of the last stage Q5 for a maximum as indicated by the scope.
6. Measure bandwidth and gain of the last stage Q5. Gain should be approximately 2.5 and the bandwidth should be greater than 4 Mc.
7. Disconnect the 360 uuf capacitor temporarily attached from collector of Q3 to ground in part 2 above.
8. Reconnect the tap of Q5 temporarily disconnected from the feedthru in part 5 above.
9. By means of a frequency counter attached to connector P2, adjust C26 of oscillator Q3 to give 60 $\pm$ .1 Mc (spec. is 0.5 mc) as indicated by the frequency counter.
10. Apply a 1.6 $V_{O.P.}$ positive pulse 16.75 u sec wide at a 3731 cps repetition rate to pin 6 and the return to pin 7 of connector P3. Observe output at P2 terminated in 50 ohms and verify that the output is blanked during the interval in which the pulse occurs.
11. While observing the same point, adjust pot R20 so that start of oscillation occurs 1 u sec after the trailing edge of the 1.6 V pulse.
12. The magnetron firing pulse normally occurs approximately .6 u sec after the trailing edge of the 1.6 V blanking pulse. By means of a pulse generator with a delay feature the Rada-Pulser, Sr. can be triggered to give a 0.5 V_{pp}, 100 n sec pulse of 60 Mc signal occurring at a point .6 u sec after blanking.

13. By using the Coho I.F. and Phase Lock Test Chassis, Unit 4A3 of the DPD-1, a verification of phase lock can be made. Connect the units according to the following sketch.



14. By observing the lock test output the locking pulse is phase compared to the coherent oscillator output (by means of a ringing delay line within the Coho I.F. and Phase Lock Test Chassis) at 12.5 u sec intervals. The lock normally is so good that in order to indicate an unlocking the frequency of the pulse must be changed by 3 Mc or more or the locking pulse must be attenuated by 30 db or more or the lock pulse must be moved by 1 microsecond or more or any combination of these things.

15. The output voltage should be IVP-P across 50Ω peak-to-peak.

I. TEST EQUIPMENT REQUIRED (or equivalent)

1.	Frequency Counter	HP 5245L
2.	Oscilloscope	Tektronix Model 585
3.	Oscilloscope Preamplifier	Tektronix Type 82
4.	IF Pulse Generator	Kay Electric, Rada-Pulser Senior
5.	Video Pulse Generator	Lavoie, Model LA-593

II. PROVIDE THE FOLLOWING VOLTAGES AND TERMINATIONS:

1.	P3-1	+ 20 VDC
2.	P3-3	- 20 VDC
3.	P3-2	Gnd
4.	P2	50 ohms

III. ELECTRICAL TEST SPECIFICATIONS

1. Frequency — 60 ± 0.5 MHz
   Measure at P2
2. Amplitude — 1 Vp-p nominal
   Measure at P2
3. Oscillator Quench

Apply the following video pulse to P3-6

Amplitude	1.6 V ± 0.3 V
Polarity	positive
Width	16.75 μs
Repetition Rate	3,731 pps (268 μs)

Quench Period Range — 17.00 μs or less to 18.25 μs or more
Measure at P2
Adjust quench period with R20

4. Phase Lock

Apply the following video pulse to P3-6

Amplitude	1.6 V ± 0.3 V
Polarity	positive
Width	16.75 μs
Repetition Rate	3,731 pps (268 μs)

Set R20 to give a 17.85 μs quench period

PREPARED BY	DATE	PREPARING ACTIVITY
F.E. Bates	5-2-69	
CHECKED BY	DATE	TITLE OR SUBJECT
		Acceptance Test Plan, COHO Assy SM-D-533217
APPROVED BY	DATE	

PHILCO
AERONUTRONIC DIVISION

PROJECT OR MODEL	
1804	
SHEET	DOCUMENT OR REPORT NO
1 or 2	40287

Apply the following signal to P1 from the Rada-Pulser

Frequency	60 ± 0.5 MHz
Pulsewidth (τ)	75 nsec
Amplitude	0.5 Vp-p
Repetition Frequency	3,731 pps (268 μs)

This signal shall be synchronized with the above 16.75 μsec video signal and appears 0.6 μsec after its trailing edge.

Phase lock is indicated by the COHO turn-on pulling into the 60 mc phase lock signal as it is applied. Pull in should be approximately 0.5 μsec. Adjust R20 to obtain this.

IV. TEST RESULTS SN # 3

Characteristic	Specification	Measured
1. Frequency	60 ± 0.5 MHz	60,000,500
2. Amplitude	1 Vp-p nominal	1.3 Vp-p
3. Quench Period Adjustment	17.00 μs to 18.25 μs min. range	16.75 M SEC
4. Phase Lock		0.5 M SEC

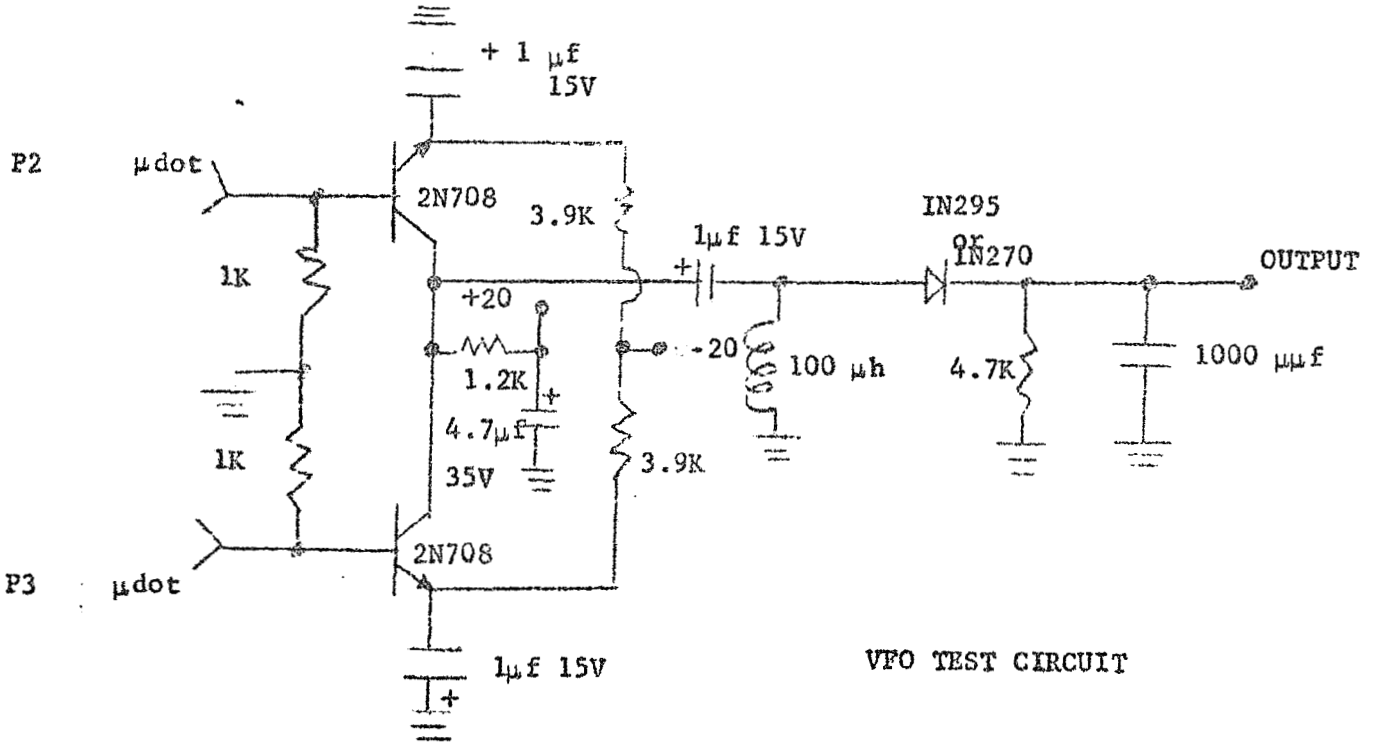
Date: 8-28-70 TEST PERFORMED BY LR Delaney

This chassis was repaired and tested under Contract No. NAS7-112??.

V. F. O. TEST (1A4A8)

1. Apply +50V to pin 6 thru a1K-3W resistor and -50V to pin 7 thru 1.6K 1W resistor and the 50V return to pin 9 of P1.
2. Ground pin 4.
2a. Set collectors of Q1 to 15V by adjusting R2 for balance and R9 for correct voltage (15V). Measure balance with Simpson VOM (between collectors) set on 50 u a scale for final setting. Use VTVM to set the 15V level.
3. Use amplifier of test jig to amplify the output out of Q3 oscillator by attaching P3 to the test jig in put.
4. Attach clip lead cable from frequency counter to collector of test jig amplifier and adjust the oscillator Q3 to a frequency of 9,996,250 cycles/sec. Remove P3 from test jig.
5. Attach P2 to the test jig input and adjust oscillator Q4 to 9,996,250 cycles/sec.
6. Attach P2 to the one input of the test jig and P3 to the other input of the test jig. Place the clip lead cable from the frequency counter across the detector load of the test jig. Attach pin 4 to the arm of the pot which is used to simulate VGOD and the return pin 5 to the ground of the pot chassis.
7. With the VGOD simulator to OV_{DC} in which case the frequency counter should indicate 0 frequency and if it is not so, a minor adjustment of one of the two oscillators should be done to make it be so.
8. Vary the VGOD simulator to $+4V_{DC}$ in which case the frequency counter* should indicate 7500 cycles/sec $\pm$ 10%. Adjust the VGOD simulator to $-4V_{DC}$ in which case the frequency counter should indicate 7500 cycles/sec $\pm$ 10%. If such is not the case, the varactors may require changing.
9. Place the VFO in the oven and apply the same power and signal to the unit. Plot a characteristic curve of the V. T. O. obtained by varying the VGOD pot from +4V to -4V and recording the frequency across the test jig detector load every .2V interval.
10. The output level of each oscillator should be greater than .02V pp.

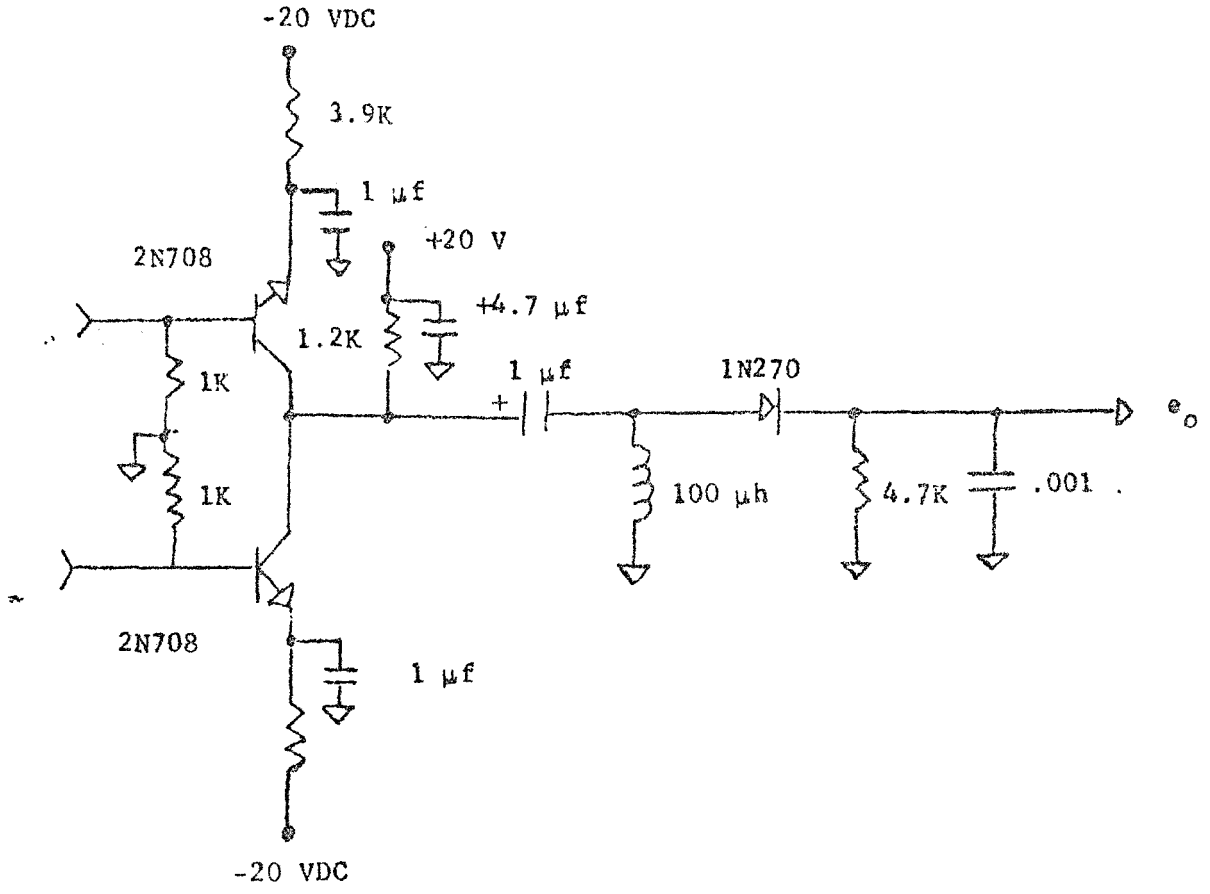
* Keep sensitivity of counter as low as possible in order to keep the ripple from causing erratic triggering of the counter which manifests itself as a



VFO TEST CIRCUIT

I. TEST EQUIPMENT REQUIRED (or equivalent)

1.	Frequency Counter	HP 5245L
2.	Oscilloscope	Tektronix Model 585
3.	Oscilloscope Preamplifier	Tektronix Model Type 82



FREQUENCY TEST CIRCUIT

PREPARED BY	DATE	PREPARING ACTIVITY
F.E. Bates	5-2-69	
CHECKED BY	DATE	TITLE OR SUBJECT

PHILCO

AERONUTRONIC DIVISION

PROJECT OR MODEL

1804

II. PROVIDE THE FOLLOWING VOLTAGES AND TERMINATIONS

1.	P1-6	+50 VDC	through 1K, 3W resistor
2.	P1-7	-50 VDC	through 1.6K, 1W resistor
3.	P1-9	Gnd	
4.	P1-4	Freq. Control, ± 4 VDC	
5.	P2	50 ohms	
6.	P3	50 ohms	

III. ELECTRICAL TEST SPECIFICATIONS

1. Amplitude 0.02 Vp-p Minimum

   Measure at P2 and P3

2. Frequency Test

   Using the Frequency Test Circuit, attach P2 and P3 to the input of the Freq. Test Circuit.

Frequency Control	Frequency Out
+4 VDC	8,370 Hz nominal
0 VDC	0 Hz nominal
-4 VDC	8,370 Hz nominal

IV. TEST RESULTS SN #3

Characteristic	Specification		Measured
1. Amplitude	0.02 Vp-p Minimum	P2	0.02 V_{p-p}
2. Frequency Output		P3	0.02 V_{p-p}
Frequency at +4 VDC control	8,370 Hz nominal		11,000 Hz
Frequency at 0 VDC control	0 Hz nominal		0
Frequency at -4 VDC	8,370 Hz nominal		10,000 Hz

Date 9-16-70 TEST PERFORMED BY LR Labanz

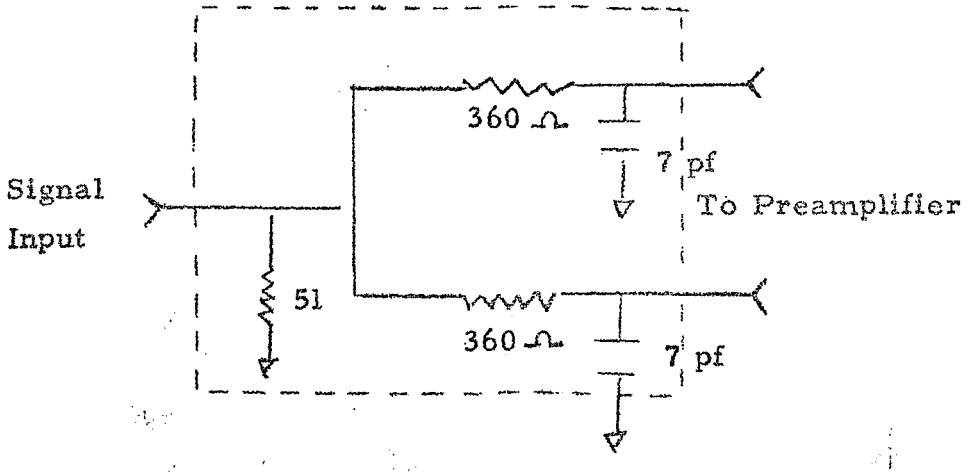
This chassis was repaired and tested under Contract No. NAS7-11278

PRE AMPLIFIER ALIGNMENT (1A2A2)

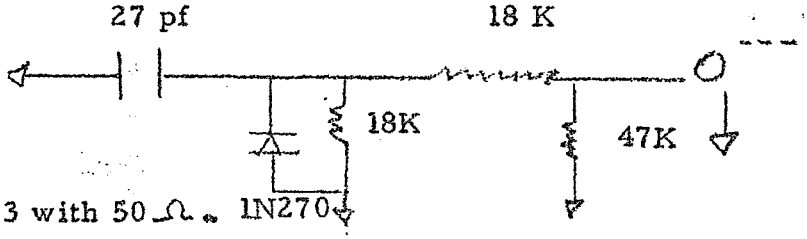
Supply the following voltages.

Pin A,	+ 200 V dc, 35 ma
Pin D,	+ 20 V dc, 5 ma
Pin E,	- 20 V dc, 5 ma
Pin C,	20 V + 200 V Return,
Pin H,	12.6 Vdc, 440 ma
Pin L,	17.6 V Return

Use the following matching pad to feed signals into the preamplifier through connector J1 and J2.

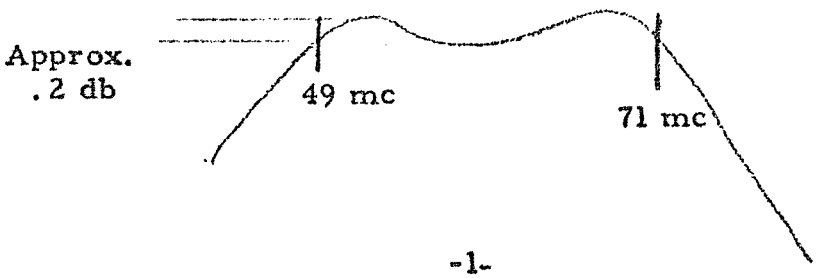


Use the following detector circuit to observe the waveforms.

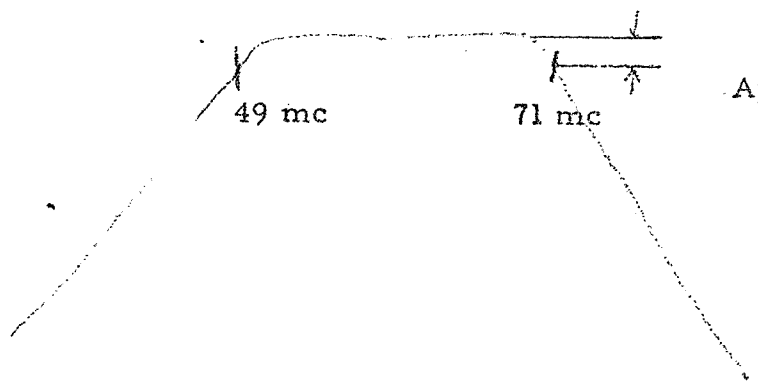


Terminate J3 with 50 Ω.

Feed a sweep signal center about 60 mc into the input through the matching pad. Observe the signal at cathode of V2. Adjust L8, L9 and L11 for a response as shown.

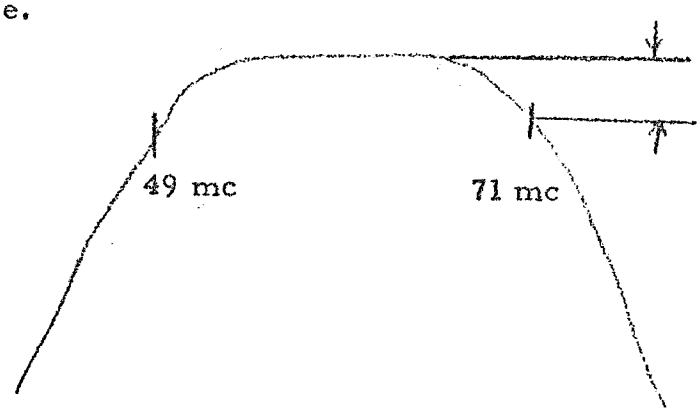


Move detector to base of Q1 and adjust C19 and C20 for the response shown.



Approximately
0.5 db down

Move detector to 50Ω load at J3 and adjust C24 and C28 for the following response.



.5 to 1 db
down @ 49 mc and 71 mc

If necessary, to meet the overall requirements, the circuits previously adjusted may be touched-up with minor adjustments.

Make a point-by-point frequency response for record.

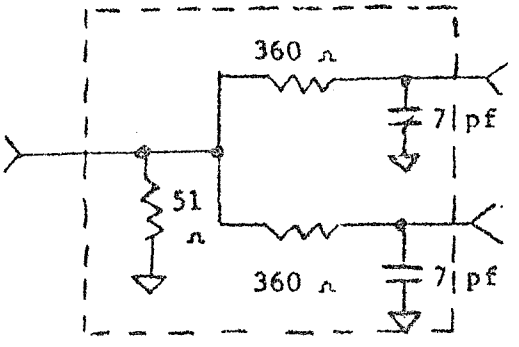
Specifications: (Including the matching network)

Bandwidth:	symmetrical about 60 mc. The top shall be reasonably flat. The response shall be down .5 to 1.0 db at 49 mc and 71 mc.
Gain :	23 db minimum (Measured through matching pad)
Noise Figure:	2 db maximum @ 60 mc (Measured without matching network)

I. TEST EQUIPMENT REQUIRED (or equivalent)

1.	Signal Generator	HP Model 608
2.	Noise Figure Meter	HP Model 340B
3.	IF Noise Source	HP Model 345A
4.	Oscilloscope	Tektronix Model 585
5.	Oscilloscope Preamplifier	Tektronic Model 82

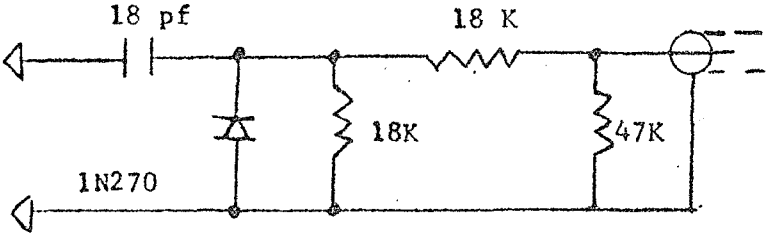
6.



To Preamplifier

Input Matching Network

7.



Detector

PREPARED BY: F.E. Bates	DATE: 5-2-69	PREPARING ACTIVITY	PHILCO AERONUTRONIC DIVISION
CHECKED BY	DATE	TITLE OR SUBJECT: Acceptance Test Plan Pre-Amp Assy	PROJECT OR MODEL: 1804

II. SUPPLY THE FOLLOWING VOLTAGES AND TERMINATIONS

1. P1-A +200 VDC (35 ma)
2. P1-D +20 VDC (5 ma)
3. P1-E -20 VDC (5 ma)
4. P1-C Gnd
5. P1-H +12.6 VDC (440 ma)
6. P1-L 12.6 V Ret
7. J3 50 Ω

III. ELECTRICAL TEST SPECIFICATIONS

Gain and Bandwidth measurements are made with matching network connected to J1 and J2. Measurements are made from input to matching network to J3

Gain	20 db min
Bandwidth	22 MHz Min. @ 1 db
Noise Figure (measured without matching network)	2 db max

IV. TEST RESULTS SN (unknown)

Characteristic	Specification	Measured
1. Gain	20 db min.	23 db
2. Bandwidth	22 MHz min. @ 1 db	22 MHZ
3. Noise Figure	2 db max.	2.0 db

DATE 9-1-70 TEST PERFORMED BY ER Gabrowski C

This chassis was repaired and tested under Contract No. NAS9-11278

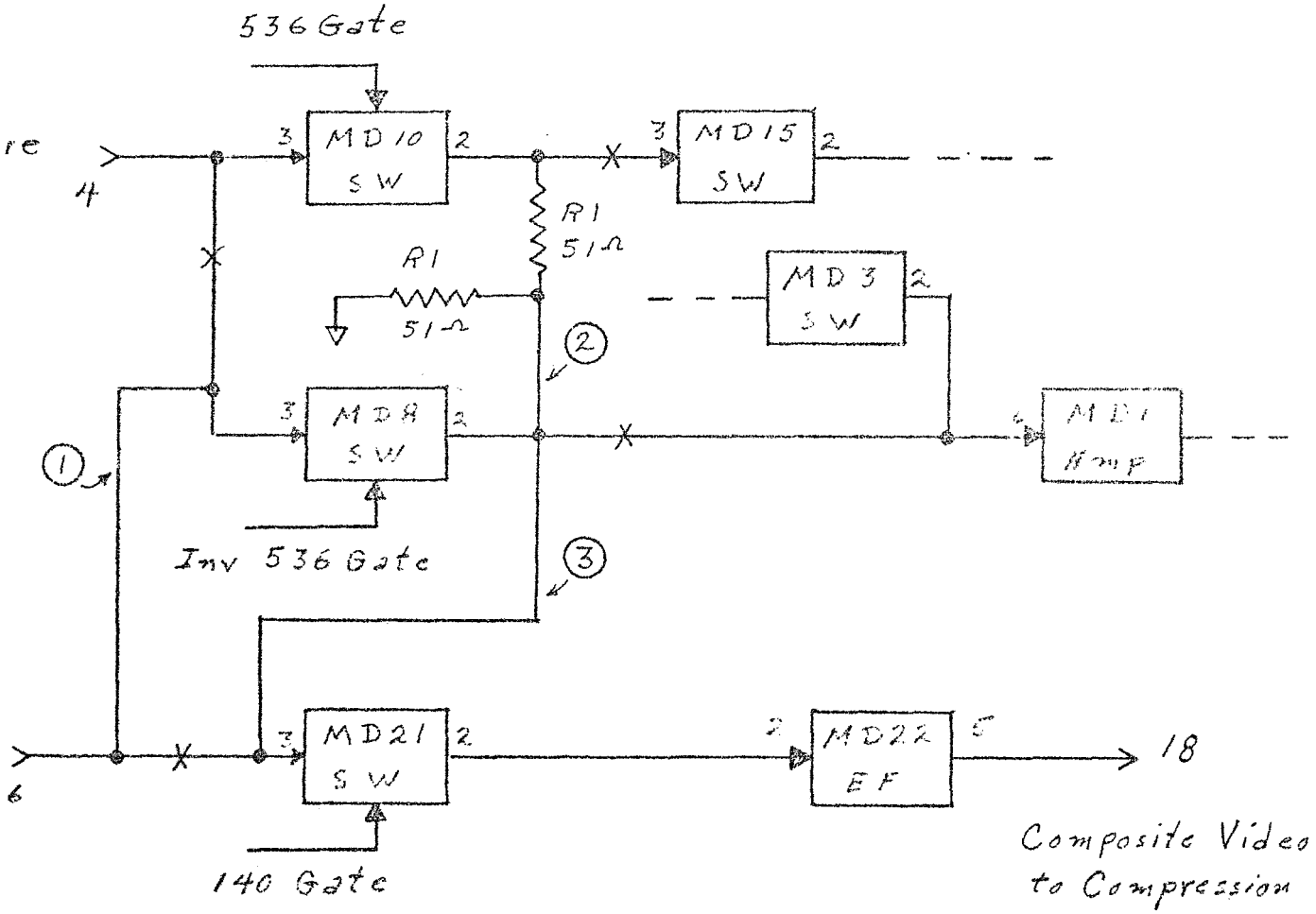
PHILCO
A SUBSIDIARY OF Ford Motor Company,
AERONUTRONIC DIVISION

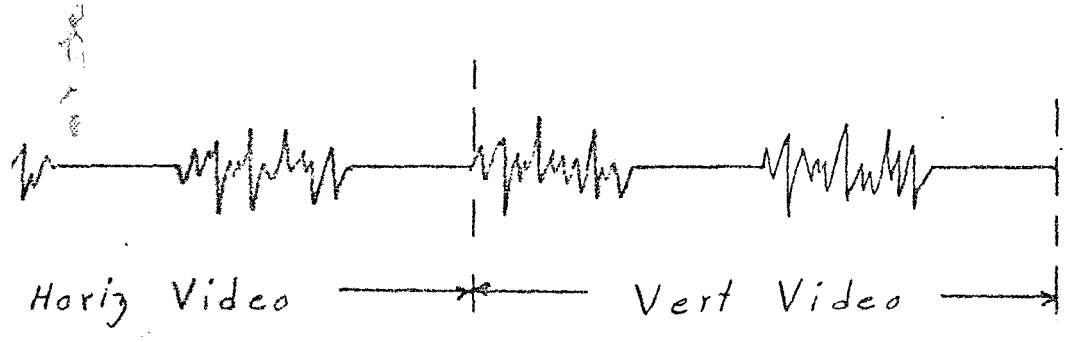
PREPARED BY	DATE	PREPARING ACTIVITY
F.E. Bates	11-26-69	
CHECKED BY	DATE	TITLE OR SUBJECT
		Processor Changes for Synthetic - Real Aperture
APPROVED BY	DATE	

PROJECT OR MODEL

SHEET OF

DOCUMENT OR REPORT NO 44231





Composite Video

Processor changes to record vertical received real aperture and horizontal received synthetic Aperture

All changes are on the CPS Board (1A6A13):

1. Open circuit at points marked 'X' (4 places)
2. Add resistors R1 and R2
3. Add wires labeled ① ② and ③

Note: R1 and R2 may require adjusting to set the level into the compression board (Approx 0.5 V p-p)